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Single Spin Wireless Architecture of nm Priority Resolver

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ABSTRACT: *Priority resolver is ubiquitous in digital logic circuits as it is frequently used to optimize large number of inputs into a minimum number of outputs. This particular circuit exclusively demonstrate manifestation of outputs, controlled by the priority of logic interventions of the inputs. CMOS Logic made circuits with higher number of inputs experiences an excessive power dissipation. On the other hand, Single Spin Logic (SSL) offers low power dissipation, high speed, high packing density in circuit design. It is a novel approach in device vicinity that involves the spin polarity of electron rather only the charge. Thus the authors motivated themselves to design SSL based priority resolver. This technical note presents a pragmatic view of priority resolver design using SSL.*

Keywords: *Not wired , power dissipation ,priority resolver , resolver , Single Spin Logic (SSL).*

I. INTRODUCTION

In modern technology, cramping of circuits has become a greatest challenge to the researchers. To achieve such requirement some technological shift has been incorporated. Few design techniques are already in use such as Carbon Nano Tubes (CNT), Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Devices (RTD), Quantum Dots (QD) , CMOS [1] and so on.

But these all are based on electron charges or conveniently these are simple charge coupled devices which suffers from leakage power. To prevail over such difficulty Prof. Supriyo Bandopadhyay of Virginia Commonwealth University conceptualized a new idea known as spintronics [2]. In spintronics, The information is carried out by using electron spin rather than electron charge. This ensures Spin degree of freedom in electronic circuits. Eventually, Sarkar et.al.[3], has applied the spin property in logic designing and a new term evolved known as 'Single Spin Logic'.

SSL has already being used in different logical circuits, such as NAND gates (H. Agarwal et.al.) [4], Full Adder (Soumitra Shukla et.al.) [5], Divider (Bahniman Ghosh et.al.) [6] and so on.

In the midst of different combinational circuits resolver is brilliant topography combining various aspects of fetching the outputs such as navigation, interrupt request control and so on. Thus a bucket full of research relevance on priority resolver is omnipresent [7].Authors here have motivated themselves to realize a priority resolver circuit by using SSL, where the output depends upon the highest prioritized input.

II. SSL BASED LOGIC REALIZATION

Digital logic family has grown up depending upon three basic gates such as NOT, AND and OR gates. The SSL based designing of the above mentioned gates are described in Fig 1a to Fig 1c.

Fig1a. SSL based NOT gate

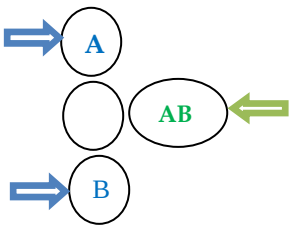

Fig1b: SSL based AND gate

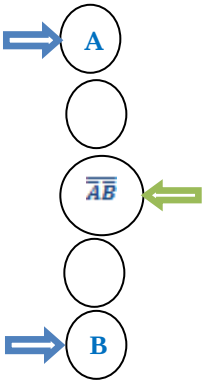

Fig1c: SSL based OR gate

In the above mentioned figures A and B are two inputs which are represented by blue arrows and corresponding outputs are represented by green arrows.

Fig 2 represent the NOT, AND and OR gates using input A as up spin (which signify logic '1') and input B as down spin(which signify logic '0')

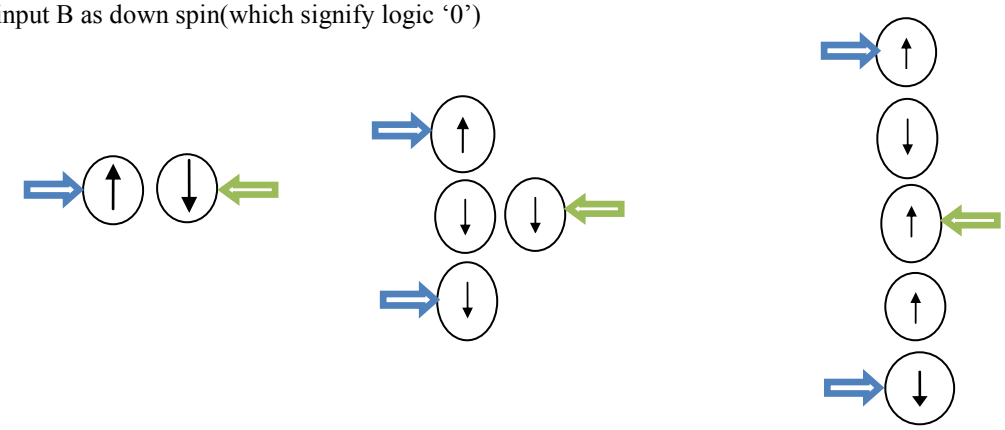

Fig2: NOT, AND, OR gate depiction for A=1 and B=0

III. PRIORITY RESOLVER

In digital electronics resolver plays a great role. Resolver selects any one inputs from it's 2n inputs and flaunt it by using its n outputs lines. In this encode users suffer from some typical problems when more than one inputs are activated. To triumph over such problems priority resolver evolves. In priority resolver the output not only depends upon the inputs but also maintain the priority (highest priority to the MSB) of the inputs. The block diagram and truth table of a 4:2 priority resolver is given in the Fig3a and Fig3b respectively.

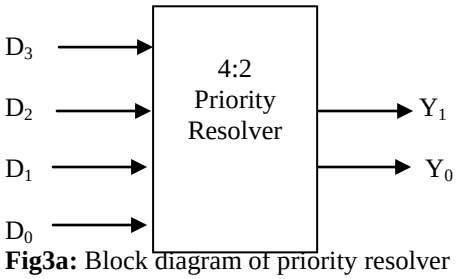

Fig3a: Block diagram of priority resolver

Inputs				Outputs	
D_3	D_2	D_1	D_0	Y_1	Y_0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

Fig3b: Truth table of priority resolver

IV. SSL BASED PRIORITY RESOLVER

The logical illustration of priority resolver is given in Fig4 where blue lines depict the inputs and green lines depict the output. In 4:2 priority resolver D_3, D_2,D_1 and D_0 are the inputs and Y_1 and Y_0 are the two inputs where $Y_1 = D_3 + D_2$ and $Y_0 = D_3 + \bar{D}_2 D_1$

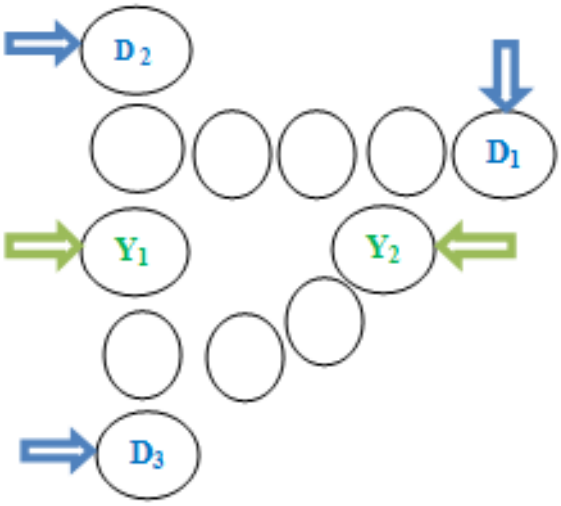

Fig4: SSL based Priority resolver

Fig5 represents the pictorial view of a priority resolver by taking some specified inputs such as $D_3 = 0$, $D_2 = 1$, $D_1 = 0$ and $D_0 = 1$.

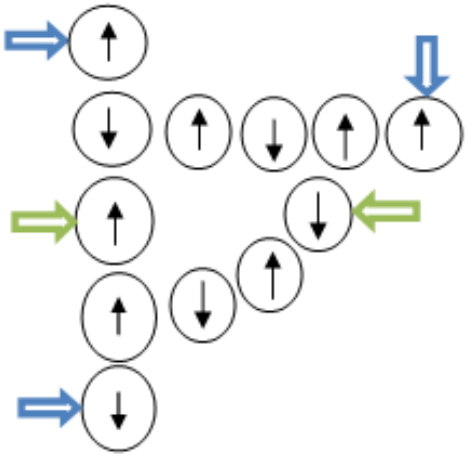

Fig5: Priority resolver using up spin and down spin representation.

V. CONCLUSION

From the above discussion we can conclude SSL based design provides fastest speed, low cost, light weight nm range ICs which can be integrated in future digital logic designing. The next generation SSL priority resolver is sure to driven out the complexities of CMOS made priority resolver.

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